WHITE PAPER

Basics of Dual Fractional-N Synthesizers/PLLs

The term fractional-N describes a family of synthesizers that allow the minimum frequency step to be a fraction of the reference frequency. Over the years, a number of methods have been proposed to realize fractional-N frequency synthesis that are based on the basic concepts of traditional integer-N synthesis [1,5].

Among these methods, three techniques are best known in the industry: fractional divider-based, current injection-based, and $\Delta\Sigma$ modulator-based fractional-N. This White Paper describes these methods and provides a general discussion of the use of fractional-N synthesizers in a low-cost, low-power radio.

Basics of Phase Locked Loops (PLLs)

A PLL is a negative feedback loop in which the phase of a generated signal is forced to follow that of a reference signal. A basic modern PLL comprises a reference source, a phase frequency detector, a charge pump, a loop filter, and a Voltage Controlled Oscillator (VCO).

The output of the VCO is phase-compared with the reference at the Phase Frequency Detector (PFD). The polarity of the measured phase difference is used to turn on the pump-up or pump-down current source in the charge pump. As a result, some charge is transferred to or taken away from the integrating capacitor in the loop filter. The amount of charge is proportional to the magnitude of the phase difference. This, in turn, results in an adjustment in the tuning voltage of the VCO so that its phase is retarded or advanced. The loop is designed so that the phase error is corrected.

The function of the PFD also ensures that it switches on the right current source (i.e., pump-up current or pump-down current) to speed up or slow down the VCO in case of a frequency difference between the two incoming signals to the PFD. When the loop reaches lock condition, the frequency of the generated signal is also equal to that of the reference.

Fundamentals of an Integer-N Frequency Synthesizer

When a frequency divider is placed between the VCO and the PFD, the PLL becomes a frequency synthesizer where the output is an integer multiple of the reference. A frequency divider is, basically, a state machine clocked by the VCO.

A rising edge occurs at the divider output every *N* number of VCO cycles. Here, *N* is a predetermined number and is referred to as the division ratio. Because the loop forces the frequency of the divider output to track that of the reference, the VCO is *N* times as fast as the reference, as illustrated by Equation 1:

$$f_{VCO} = N \times f_{ref} \quad (1)$$

where: f_{VCO} = output frequency of the VCO
f_{ref} = the reference frequency

Equation 1 indicates that a frequency synthesizer can be viewed as a frequency multiplier with its input and output frequency related.

If the frequency division ratio is programmable, an integer-N frequency synthesizer is formed as illustrated in Figure 1. A programmable divider is a loadable digital counter. Its output completes a cycle every *N* VCO cycles, much like a simple frequency divider.

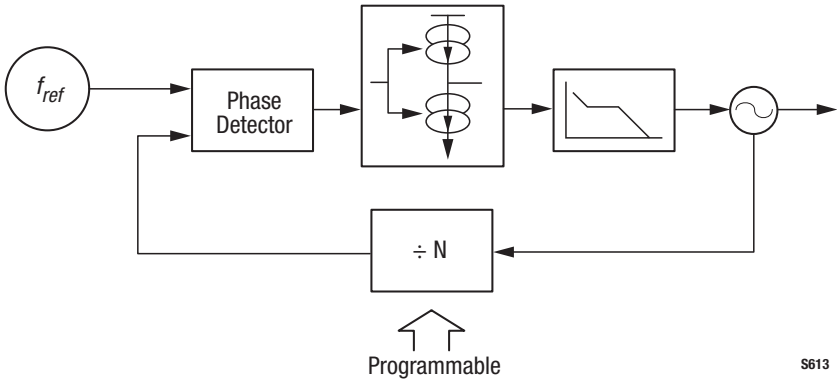

Figure 1. Basic Integer-N Synthesizer Architecture

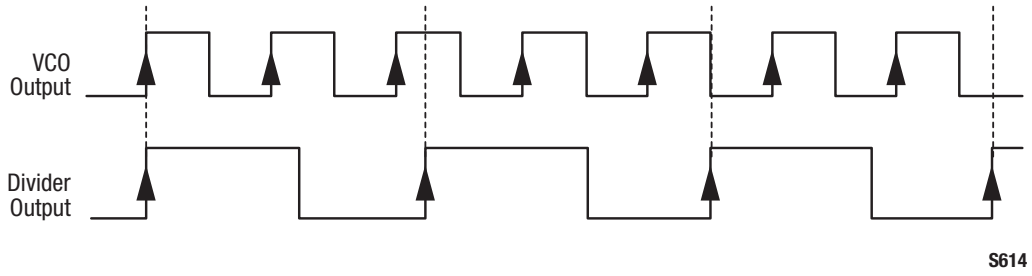

Figure 2. Timing Diagram of a Fractional-N Frequency Divider

Since the division ratio is programmable, the output frequency (f_{vco}) can be changed by programming *N* to a new value. Note that the synthesizable frequencies can only be integer multiples of the input reference frequency (therefore, the name "integer-N synthesizer"). As a result, the minimum channel spacing, or frequency step size, is equal to f_{ref}. This is a primary constraint of integer-N synthesizers.

Fractional-N Frequency Synthesis

The frequency synthesized by a fractional-N synthesizer can be a non-integer multiple of the reference, as illustrated by the following equation:

$$f_{VCO} = \left(N + \frac{k}{M} \right) \times f_{ref}$$

where *k* and *M* are integers

The variable *M* is a measure of the fractionality that a fractional-N synthesizer can provide. It is usually referred to as "fractional modulus" or "fractional denominator." The integer number *k* can assume any number between 0 and *M*. The non-integer number (*N + k/M*) is often written as *N.F*, where the dot denotes a decimal point, and *N* and *F* represent the integer and fractional parts of the number, respectively.

Traditional fractional-N synthesis methods are based on the basic concepts of integer N synthesis [1,5]. The three most common methods – fractional divider-based, current injection-based, and $\Delta\Sigma$ modulator-based – are described below. The last two methods are based on the concept of division ratio averaging.

Fractional Divider-Based Fractional-N

This technique evolves from the fundamental principles of integer-N synthesis. The only difference is that the frequency divider is replaced with a fractional divider. A fractional frequency divider is no longer a simple digital counter. The period of the divider output (T_{do}) is given by the following equation:

$$T_{do} = (N + 0.F) \times T_{vco}$$

where: *0.F* = a fractional number
T_{vco} = the period of the VCO

It's important to mention that once *N* and *0.F* are set, the period of a fractional divider output is ideally not time varying. In other words, a rising edge occurs at the output each *N* and *0.F* VCO cycle. The timing diagram in Figure 2 illustrates the operation of a fractional divider where *N.F* is equal to 2.25.

As with the case of an integer-N synthesizer, T_{do} is forced to follow the reference period. Therefore,

$$T_{ref} = (N + 0.F) \times T_{vco}$$

or:

$$f_{VCO} = (N + 0.F) \times f_{ref}$$

where T_{ref} is the reference period.

A simple fractional frequency divider circuit is shown in Figure 3. This block diagram shows a divider comprised of a Dual Modulus Divider (DMD), a Delay Locked Loop (DLL), a Multiplexer (MUX), and a Digital Phase Accumulator (DPA). Note, however, that a fractional divider does not have to be based on a DLL [6].

The DLL shown in Figure 4 consists of a set of cascaded, tunable, delay elements; a phase detector; a charge pump; and a D-type flip-flop. The negative nature of the feedback in the DLL ensures that the total delay through the delay line is one VCO cycle. Since the delay elements are, ideally, identical, a VCO period is broken up into N_d equal packets of phase, where N_d is the number of delay elements in the delay line.

A simple DPA is made up of an adder and a register, as illustrated in Figure 4. The register is clocked by the reference. The input to the DPA is an *m*-bit word. The contents of the register are used to control the MUX. On every reference rising edge, the contents are incremented by the value of the input, *x*, which is represented by an *m* bits word. The output of the DPA (i.e., the carry-out of the adder) is a one-bit quantization of the input.

The number of bits in the accumulator (*m*) is related to the number of discrete packets of phase by the following equation:

$$N_d = 2^m$$

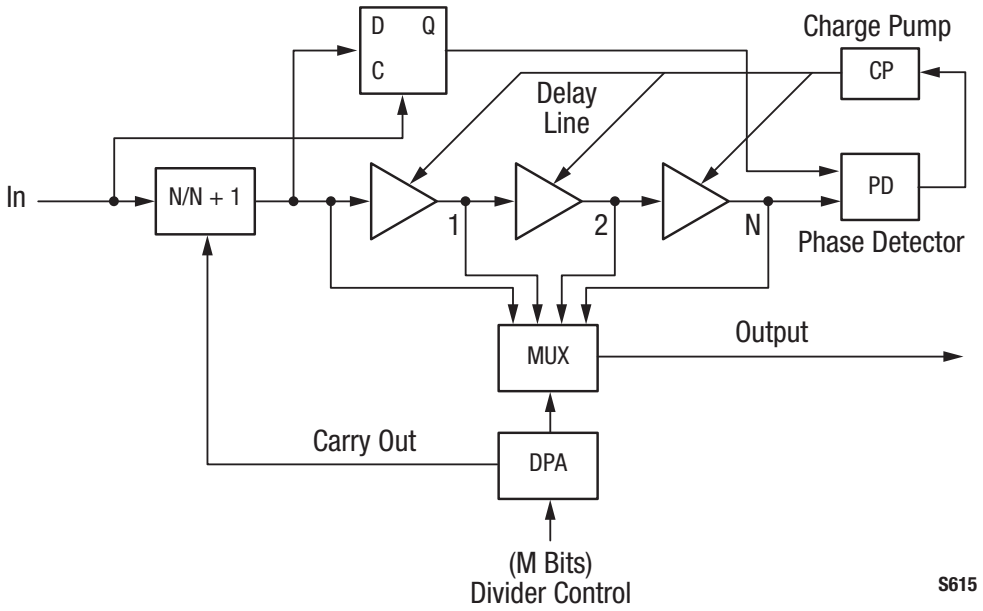

Figure 3. Example of Fractional-N Divider Implementation

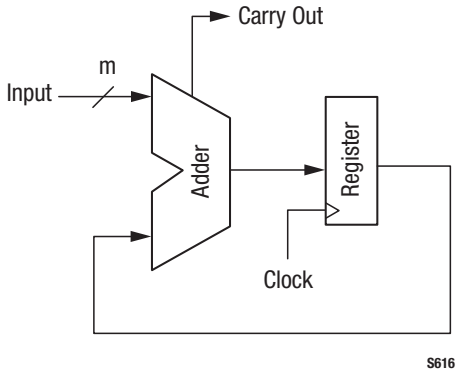

Figure 4. Design of a Simple Digital Phase Accumulator

The output of the DPA controls the DMD. When carry-out is high, the DMD divides by $N + 1$ as opposed to N when carry-out is low. In the following example, the fractional division ratio, $N + 0.F$, for a DPA input of x, is equal to $N + x/2^m$.

Suppose the DPA has three bits and, therefore, the delay line has eight elements. Each phase packet corresponds to 1/8 of a VCO cycle. Also, assume that the input is equal to 2, which corresponds to a $0.F$ of 2/8. When no carry-out occurs, the DMD divides by N. Its output, however, is not immediately presented to the PFD of the PLL. Rather, it is delayed by a number of phase packets controlled or selected by the MUX. This number is equal to the content of the DPA, which is incremented by 2 every reference cycle. This means that the output is phase-shifted by a progressively increasing number of phase packets (i.e., 0, 2, 4, 6, 8) each reference cycle. As a result, the period of the DMD output is increased by 2/8 of a VCO cycle. Therefore, the effective division ratio becomes $N + 0.25$, which is what it should be.

When the DPA content reaches 8, the content of the DPA is reset, and the output of the DMD is not delayed by the delay line. However, this coincides with a carry-out, which forces the DMD to divide by $N + 1$. This is equivalent to the DMD dividing by N and its output being delayed by 8 phase packets (i.e., one VCO cycle).

The design of the fractional divider dictates the fractional modulus or fractional denominator to be N_d, the number of delay elements. Because all the elements in the delay line operate at the VCO speed, the added power consumption can be significant, especially when the VCO frequency and/or fractionality is high. Another drawback of this method is that the edges of the fractional divider output may be noisy as a result of jitter on the

outputs of the delay elements. Jitter is present due to mismatch and phase error from the phase error-correcting action of the DLL. The edge contamination may result in a significant increase in the phase detector noise floor.

Averaging Fractional-N

Another way to achieve fractional-N synthesis is through division-ratio averaging. The idea is that an integer frequency divider, as opposed to a fractional divider, is used but the division ratio is dynamically switched between two or more values. Effectively, the divider divides by a non-integer number. This number is determined by the values among which the division ratio is changed and the probability of each division ratio used.

For example, if the divider divides by 100 half of the time and by 101 the other half of the time, the average division ratio is 100.5. In general, the non-integer division ratio is given by the following equation:

$$N.F = N_1P_1 + N_2P_2 + ...N_jN_j$$

where *N.F* denotes the average division ratio, and N_i and P_i are the integer division ratio and the probabilities associated with them, respectively. Again, since the average divider output frequency is equal to f_{ref}, the following relationship exists when the loop is in lock:

$$f_{VCO} = N.F \times f_{ref}$$

One way to switch the division ratio dynamically is through the use of a simple modulus controller. A modulus controller can be a simple DPA. The output of the DPA is used to control the division ratio of a DMD. The divider divides by *N + 1* when there is a carry-out and by *N*, otherwise. In this case, the fractional part of the average division ratio is equal to the input to the DPA.

This statement can be proven as follows. First, the average value of the DPA output is equal to its input, which is the way a DPA works. This average is also equal to the probability of the DPA carry-out being a 1. Knowing this probability, *p*, the average division ratio, can be readily calculated as:

$$N.F = N + p$$

where *p* is related to the input of the DPA by:

$$p = \frac{x}{2^m}$$

Note that the input of the DPA (*x*) is represented by an m-bit word.

It can be shown that a DPA, as depicted in Figure 4, is actually a first-order ΔΣ modulator. Like any ΔΣ modulator, the output of a DPA exhibits quantization errors. How quantization errors result in quantization phase errors, and what to do with them, is discussed below.

In general, there are two ways to deal with quantization phase errors: cancellation by current injection or ΔΣ noise shaping.

These two techniques lead to two different types of averaging fractional-N synthesis, the current injection-based fractional-N and ΔΣ fractional-N.

Quantization Phase Error

The information presented here is based on a DPA-controlled, dual-modulus divider. To facilitate the definition, imagine an ideal fractional frequency divider that divides by *N.F*. Here, ideal means that the period of the imaginary divider output is always *N.F* VCO cycles, precisely. It adds no noise or jitter to its output.

Quantization error in the DPA output exists because the output is an approximation of the input and is never equal to the desired value. This is simply because the output is either 0 or 1, while the input is between 0 and 1 (excluding 0 and 1).

Accordingly, the instantaneous division ratio of the DMD is never equal to the average division ratio by which the imaginary divider divides. This, in turn, gives rise to a phase difference between the actual instantaneous DMD output and the imaginary divider output. If the latter is viewed as a reference, then the former exhibits phase error with respect to the latter. This phase error is defined as quantization phase error or quantization phase noise. It is also referred to as quantization noise for simplicity.

There are two points worth mentioning. First, the imaginary divider output is phase-locked to the reference. The phase difference between the two signals is such that there is no error correction signal at the output of the charge pump. Secondly, the waveform of the actual DMD output can be viewed as the imaginary divider output with its phase being modified by the quantization phase error. With this understanding, the DPA-controlled DMD can be modeled as an ideal fractional divider plus a quantization noise source, as illustrated in Figure 5.

Figure 5 can be used to derive the transfer function for the quantization phase error in the s domain (i.e., the transfer function from this phase error source to the VCO output). This function can be defined as Equation 2:

$$\Phi_{q,o}(s) = \left[\frac{(N.F \times K_{cp} \times K_{vco}) \times F_{(s)}}{(N.F \times s) + F_{(s)} \times (K_{cp} \times K_{vco})} \right] \times \Phi_q(s) \quad (2)$$

where: $\Phi_{q,o}(s)$ =output quantization noise.
$\Phi_q(s)$ = input quantization noise.
$F(s)$ = impedance of the loop filter.
K_{cp} = charge pump gain.
K_{vco} = VCO sensitivity.

Note that other noise sources are not illustrated in Figure 5. These include the phase noise on the reference, noise due to the CP/PD, VCO noise, and random noise due to the divider.

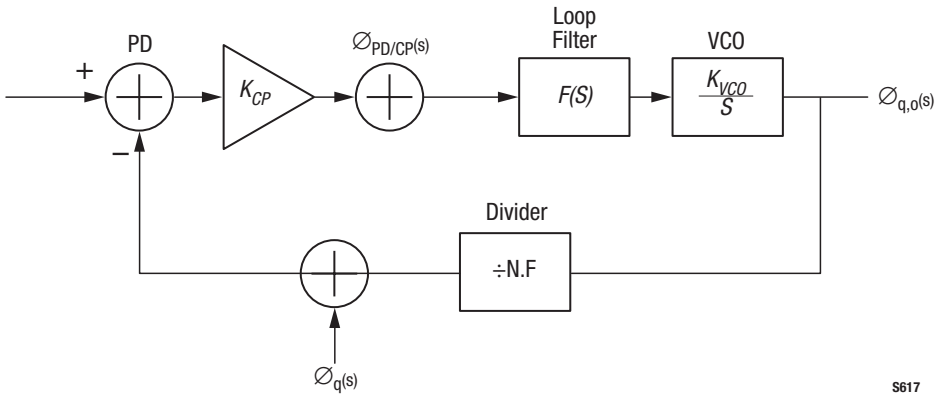

Figure 5. A Linearized Phase-Domain Model of a PLL With Quantization Noise Source

The quantization phase error causes phase error at the PFD. The waveform of the phase error sensed by the PFD is the quantization phase error with, possibly, some DC offset. The phase error at the PFD gives rise to a current signal at the charge pump output. The current waveform is a scaled version of the phase error with the scaling factor being the charge pump gain. The current signal is converted to a voltage signal by the loop filter. The latter modulates the instantaneous frequency of the VCO.

If the quantization phase error waveform exhibits some periodicity and if the magnitude of the waveform is large, it shows up in the voltage signal as well. As a consequence, the VCO is modulated periodically, which causes spurs in the VCO spectrum at the offset frequency corresponding to the periodicity of the current waveform and its harmonics.

To show the periodicity of the quantization phase error waveform, the relationship between the DPA output and the quantization phase error must be derived.

Suppose that at the present reference cycle, the DMD divides by *N*. This means that the present DMD cycle is shorter than one period of the imaginary divider by $(N.F - N)T_{vco}$. That is, the phase error, in radians, changes by:

$$\frac{(N.F - N)(T_{VCO} \times 2\pi)}{(N.F \times T_{VCO})} = \frac{(N.F - N) \times 2\pi}{N.F}$$

Here, a convention is assumed: when the imaginary divider output leads the actual DMD output, the sign of the phase error is positive. If the DMD divides by $N + 1$, the DMD cycle is longer than one imaginary cycle by $(N + 1 - N.F)T_{vco}$. This corresponds to a change in the phase error by:

$$\frac{-(N + 1 - N.F) \times 2\pi}{N.F} = \frac{(N.F - N - 1) \times 2\pi}{N.F}$$

Regardless of the DPA output, the phase error changes by:

$$\frac{(N.F - N_i) \times 2\pi}{N.F}$$

where N_i is the DPA output for the present reference cycle. Therefore, the instantaneous quantization phase error, Φ, is related to N_i by the relationship defined by Equation 3:

$$\Phi = \left(\frac{2\pi}{N.F}\right)(\sum i)(N.F - N_i) \qquad (3)$$

This equation indicates that the quantization phase error is a time-integrated and scaled version of the DPA output. It can be seen that the output waveform of a DPA exhibits a periodicity of $f_{ref}0.F$. This is because, on average, every $1/0.F$ reference cycles, a carry-out occurs (i.e., the DPA outputs a 1).

According to Equation 3, the quantization phase error waveform exhibits the same periodicity as the DPA output waveform. Figure 6 shows a quantization phase error waveform together with its corresponding DPA output waveform, where $0.F$ is equal to 0.25.

A couple of observations regarding Figure 6 are worth making. The DPA output stays low for three consecutive cycles every four reference cycles. During these three cycles, the actual DMD output lags the imaginary divider output, causing the quantization phase error to grow continuously. On the subsequent fourth cycle, the phase error returns to its minimum level. It then starts to ramp up again. As a result, the quantization phase error is a repetitive ramp waveform.

Referring to the previous discussion on the effect of periodicity in the quantization phase error waveform, it's known that this causes spurs in the VCO spectrum at offset frequencies of $\pm f_{ref}0.F$, $\pm 2f_{ref}0.F$, $\pm 3f_{ref}0.F$, etc. Since these spurs occur at multiples of $f_{ref}0.F$ with $0.F$ being the fractional part of the average division ratio, they are called fractional spurs.

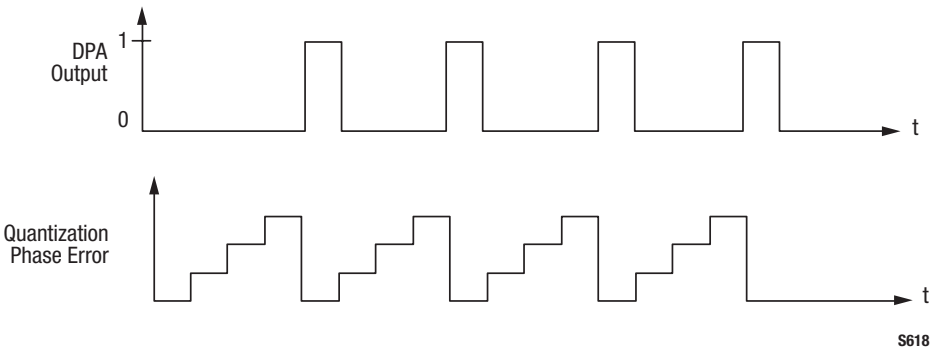

Figure 6. A DMD Output Waveform and its Corresponding Quantization Phase Error

Current Injection-Based Fractional Compensation

The fractional spurs in the above-mentioned averaging fractional-N synthesis are a serious problem. The magnitude of the periodic waveform of the resulting quantization phase error waveform is large compared to random jitters on the DMD output or the reference, yielding fractional spurs typically only 20 to 30 dB below the carrier [2]. As a consequence, various methods of suppressing these spurs have been devised [1, 7].

Returning to the derivation of Equation 3, notice that the quantization phase error changes by a well-defined amount every reference cycle. If a current pulse train can be injected with the same width but opposite sign to the integrating capacitor in the loop filter, the quantization phase error can be ideally cancelled. This is called fractional compensation.

Usually, mismatches exist between the amplitude and width of the compensation current and those of the charge pump, and therefore, cancellation of the quantization phase error is imperfect. As a result, fractional spurs can still be quite large.

There is an important point to note when current injection-based, fractional-N is compared with fractional division. Fractional frequency division is commonly viewed as a method of fractional compensation. In this view, the fractional divider is broken into two parts: a DPA-controlled DMD and DLL-based phase error cancellation circuitry. The quantization phase error introduced by the DPA-controlled DMD is cancelled before it is presented to the PFD. This way, no current injection is needed, ideally.

ΔΣ Noise Shaping

To understand ΔΣ noise shaping, it's necessary to move from the time domain to the frequency domain. A quantization phase error waveform has a corresponding frequency domain spectrum.

Initially, it's important to understand the spectrum of the quantization phase error produced by a DPA-controlled DMD.

Referring to the previous discussion about the waveform of this phase error, the spectrum has large-amplitude components at multiples of *0.F*. In other words, most of the energy appears at, or around, these frequencies.

The idea of using ΔΣ noise shaping is to first distribute, or spread, the energy in these tones evenly across some frequency range and then push the energy in the low frequencies to high frequencies. This can be accomplished by using a high-order ΔΣ modulator to control the dual (or multiple) modulus divider. For simplicity, the term ΔΣ, as used in this White Paper, is intended to mean high order, typically fourth order.

The spread of energy in the large tones is because the periodicity in a simple DPA output is destroyed when moving to a ΔΣ modulator. Figure 7 shows a waveform of quantization phase error where the input to the modulator is equal to 0.25, the clock frequency is at 25 MHz, and the integer part of the division ratio is 100. Its corresponding quantization noise spectrum is illustrated in Figure 8. The two diagrams clearly show that the periodicity seen in Figure 6 is reduced.

Correspondingly, the quantization phase noise spectrum has no large tones in its spectrum. Also, the energy in the quantization noise is moved to high frequencies due to noise shaping.

Finally, it's important to point out that the quantization phase noise for an nth order ΔΣ modulator only exhibits an n – 1 order of noise-shaping characteristic. This is because the quantization phase error is a time-integrated version of the modulator output (see Equation 2). The quantization noise spectrum illustrated in Figure 8 is for a fourth-order ΔΣ modulator. The modulator, however, only has a roll-off of 60 dB per decade.

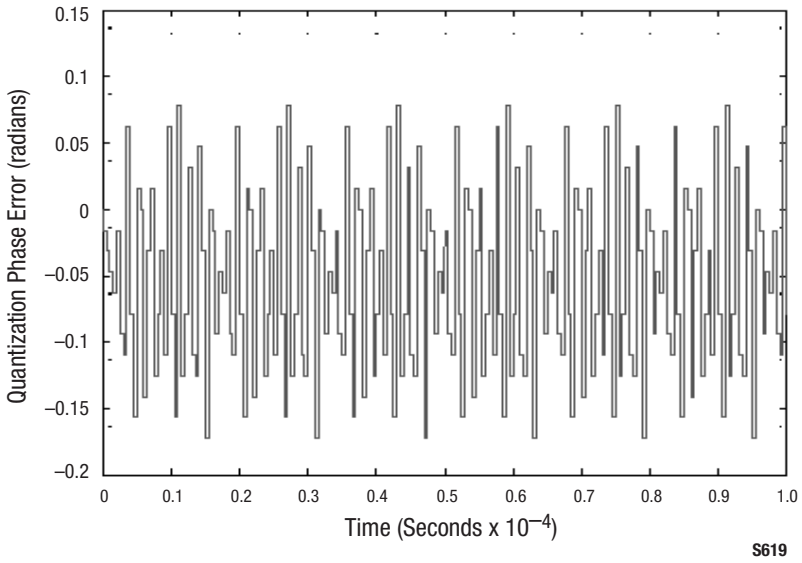

Figure 7. Quantization Phase Error for a 4th Order ΔΣ Modulator

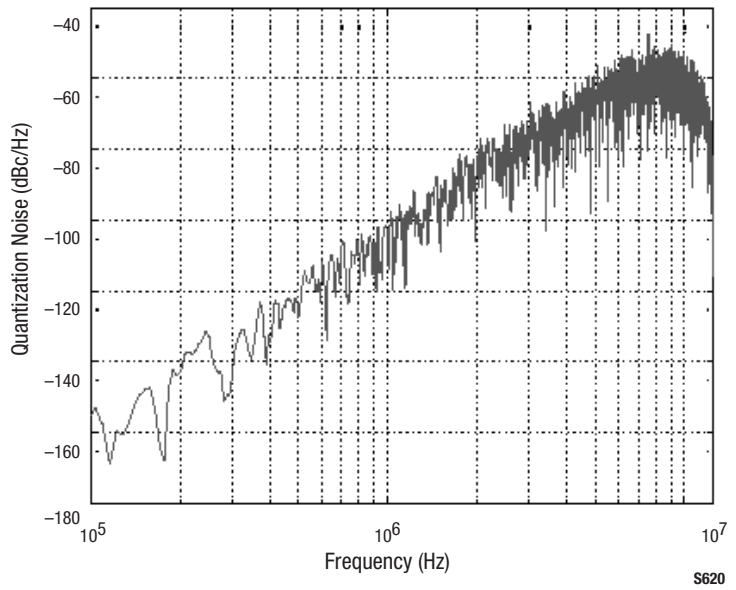

Figure 8. Quantization Phase Noise Spectrum Corresponding to the Waveform in Figure 7

Quantization Noise Attenuation and Loop Filter Design Consideration

It was previously noted that a ΔΣ modulator-controlled DMD or Multiple Modulus Divider (MMD) can be modeled as an ideal fractional frequency divider plus a quantization noise source (see Figure 5). In other words, the ΔΣ modulator and DMD or MMD, as a whole, inject quantization noise into the PLL just as other blocks introduce random noise.

The high-frequency quantization noise illustrated in Figure 8 can result in unacceptably high phase noise in the synthesizer spectrum if the loop filter is not well designed. According to Equation 2, the transfer function for quantization noise exhibits a low-pass characteristic just like the one for phase noise on the reference. Therefore, quantization noise outside the loop bandwidth can be attenuated by the low-pass filtering function of the loop. Inside the loop bandwidth, the quantization noise is low enough not to affect the overall phase noise due to noise shaping.

The key to ΔΣ fractional-N loop filter design is to ensure that quantization noise at high frequencies is sufficiently attenuated. In the case where a wide loop bandwidth is required, one or two poles need to be added to a typical one-zero, two-pole loop filter. The two added poles should not be close enough to the existing, lower-frequency pole to affect loop stability.

Traditional Integer-N Synthesizer Trade-Offs

Performance Parameters of Frequency Synthesizers

In terms of performance, the important parameters of a synthesizer include phase noise, frequency step size or frequency resolution, tuning speed or channel switching speed, spur size, and operating frequency range. Other important parameters include current consumption, power supply voltage, cost, package size, pin count, etc.

This section describes the major trade-offs in integer-N frequency synthesis. A good understanding of these trade-offs should help to appreciate the benefits of fractional-N synthesizers.

Trade-Offs Between Step Size and Tuning Speed

In integer N synthesizers, the step size is tied to the reference frequency. A small step size requires a low f_{ref}. However, the loop bandwidth is limited by the reference frequency. The loop bandwidth should be sufficiently lower than f_{ref} to keep the reference feedthrough low.

As a general rule, the loop bandwidth should be at least 10 times lower than the reference frequency to avoid the sampling effect of the PFD. Therefore, the smaller the step size, the narrower the loop bandwidth. However, loop bandwidth is the primary factor used to determine tuning speed. Generally, the wider the loop bandwidth, the faster the channel switching speed. Therefore, small step size conflicts with fast loop response unless high reference feedthrough spurs can be tolerated.

Trade-offs Between Step Size and Phase Noise

Phase noise at a given offset frequency is determined by the in-band phase noise floor and the loop bandwidth. At a fixed offset frequency, phase noise can be lowered by narrowing loop bandwidth (i.e., at the cost of a slower channel switching speed). The in-band phase noise floor is mainly determined by two factors: the input-referred phase detector/charge pump noise and the frequency division ratio, *N*. The relationship between these factors can be expressed by Equation 4:

$$P = PD_i + 20 \log N \quad (4)$$

where: P = Phase noise floor
PD_i = Input-referred phase detector/charge pump noise floor

The input-referred phase detector/charge pump noise is the same noise that occurs when back-referenced to the input of the phase detector. This way, the phase detector/charge pump noise sources are moved to the input of the phase detector and are treated as a phase noise on the reference, while the phase detector and charge pump, themselves, are left noise-free.

Around the PLL, each building block contributes to the in-band phase noise. In theory, this noise is a sum of the following:

- Multiplied reference phase noise
- Multiplied input-referred phase detector/charge pump phase noise
- Multiplied quantization noise
- Suppressed VCO noise
- Phase noise contribution from the divider

The meaning of the first three sources of noise is explained further in this document.

In modern frequency synthesizers, the contribution from a phase detector/charge pump usually dominates that from other noise sources inside the loop bandwidth. Consequently, only the phase detector/charge pump noise contribution appears in Equation (4).

It is well known that inside the loop bandwidth, the phase noise on the reference (in radians) is multiplied by *N* when it appears in the spectrum of the output. This is because the phase noise on the reference (in time) is forced to be equal to the phase noise on the VCO output (in time) while the reference period is *N* times as long as the VCO period.

The law of multiplication by *N* holds for input-referred phase detector/charge pump noise and quantization noise as well. This law simply states that for a fixed VCO frequency, the phase noise floor goes down by 6 dB for every doubling of reference frequency. However, in the real world, this is often not the case. The reason is that the input-referred phase detector/charge pump

noise floor can also be dependent on f_{ref}. In fact, it goes up with increasing f_{ref}. As a result, a 6 dB decrease in phase noise floor for every doubling of f_{ref} might not be attained. In some synthesizers, the improvement is only about 3 dB.

This shows that the phase noise floor conflicts with the step size. This conflict can be somewhat mitigated by choosing a narrow loop bandwidth. However, the loop bandwidth cannot be infinitely small. Otherwise, the loop is susceptible to mechanical vibration and other disturbances such as variation on power supply and VCO load pulling. Also, narrow loop bandwidth means slow channel switching speed.

Trade-Off Between Step Size and Reference Feedthrough Spurs

There are two reasons for a step size and reference feedthrough trade-off. The first reason has to do with tuning speed or loop bandwidth. For a given loop bandwidth, the higher the reference frequency, the lower the feedthrough spurs. The second reason has to do with various leakages through the charge pump (as a result of finite output impedance), capacitors in the loop filter, and the VCO capacitor.

At low reference frequencies, a typical charge pump outputs short, alternating pulses of current with long periods in between in which the charge pump is tri-stated. The various leakages cause a modulating signal in the VCO tuning line. The key point here is that the amplitude of the modulation signal increases with decreasing f_{ref}. Therefore, the lower the reference frequency, the higher the reference feedthrough spurs if leakage is the dominating cause of the spurs.

It is believed that at low reference frequencies (e.g., around or less than 30 kHz), leakage is the dominant cause of spurs [8].

Summary of the Integer-N Synthesizer Trade-Offs

Figure 9 summarizes the integer-N synthesizer trade-offs. Performance parameters are placed in circles while intermediate parameters are inside rectangles.

The intermediate parameter phase noise floor, as defined in this White Paper, is exclusively determined by the input-referred phase detector/charge pump noise floor and the frequency division ratio *N*. Phase noise, or more specifically phase noise at given offset frequencies, can be affected by the loop bandwidth besides the phase noise floor.

Each of the four performance parameters shown in Figure 9 is assigned an arrow with a unique shape and a given direction. The directions of the arrows indicate the desired performance. Arrows that point up represent high, large, fast, and wide. Arrows that point down symbolize low, small, slow, and narrow. For example, small reference feedthrough spurs are desirable, so an arrow that points down has been assigned to this in Figure 9.

Each performance arrow has an image arrow in its neighboring intermediate-parameter rectangle. The image arrow has the same shape as its original. The direction of the image arrow represents the requirement of the desired performance of the original parameter on the corresponding intermediate parameter. For example, fast tuning speed requires a large-loop bandwidth. Therefore, the image of the tuning speed arrow in the loop bandwidth rectangle also points up. As another example, the image of the down arrow for reference feedthrough spurs points up. The change in the arrow direction reflects the fact that low feedthrough spurs require relatively high reference frequencies.

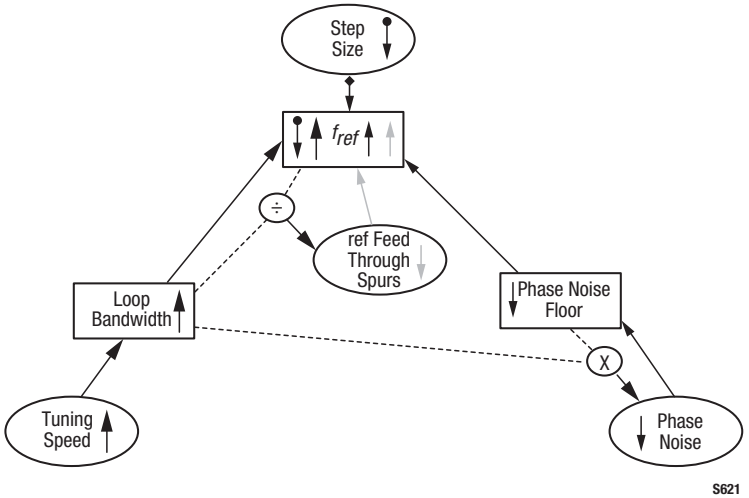

Figure 9. A Performance Parameter Summary

The image arrows can have "child" image arrows in neighboring intermediate parameter rectangles, just as the performance parameter arrows have image arrows. Again, the shape of the "child" image arrow is the same as the corresponding parent image arrow while they may be different in direction. For example, the loop bandwidth arrow that points up has a "child" image in the f_{ref} rectangle with the same direction because large loop bandwidths require a high f_{ref}. Likewise, the phase noise floor arrow that points down has an image in the same rectangle with an opposite direction.

The multiplication symbol generally indicates that the phase noise spectrum is the result of the phase noise floor being multiplied by the closed loop transfer function. The division symbol with an arrow pointing to the "ref Feed Through Spurs" process symbolizes that the spur size is affected by how far away the spur is from the boundary of the pass band of the closed loop transfer function.

Trade-offs mentioned earlier are reflected by the four arrows in the f_{ref} rectangle. In this rectangle, the arrow corresponding to the step size points down while the other three, which are the image or grand images of the other three performance parameters, point up.

With integer-N frequency synthesis, it is relatively easy to achieve good performance on any single parameter if the other parameters are disregarded. Also, the following combinations of performance benefits can be achieved at certain costs:

- Small step size and low phase noise (at least at relatively high offset frequencies) at the cost of slow tuning speed.
- Fast tuning speed and low phase noise if large step size is allowed.
- Fast tuning speed and moderately small step size at the cost of high reference feedthrough spurs. However, it is difficult if not impossible, to have small step size, fast tuning speed, low phase noise, and low feedthrough spurs at the same time.

The Advantages of Fractional-N Synthesizers

A close examination of Figure 9 shows that if the tie between step size and f_{ref} can be cut so that both small step size and high f_{ref} can exist at the same time, the previously mentioned trade-offs are eliminated. That is, if the arrow that points up in the f_{ref} rectangle is removed, there are no conflicting performance parameters. This is exactly what fractional-N synthesizers do.

In fractional-N synthesis, especially with $\Delta\Sigma$ fractional-N, the choice of the reference frequency is almost completely independent of the step size since the latter is related to the former by the following relationship:

$$Step\ size = \frac{f_{ref}}{2^m}$$

where the exponent, m, is the number of bits in the input of the $\Delta\Sigma$ modulator. For example, if f_{ref} is 25 MHz, with m equal to 20 bits, a step size as small as 23.8 Hz can be achieved.

Obviously, the benefit of fractional-N is that all the desirable performance parameters (i.e., low phase noise, low-reference feedthrough spurs, fast tuning speed, and small step size) can be achieved at the same time, at least in theory.

Low phase noise is simply the result of a high reference frequency. With $\Delta\Sigma$ fractional-N, the reference can be tens of MHz. Therefore, reference feedthrough spurs are simply not an issue at all. Also, the step size can be arbitrarily small. For example, a step size of less than 1 Hz has been reported while using a high f_{ref} [9]. Tuning speed is increased because of a widened loop bandwidth. It can be further improved with the addition of some form of pre-tuning or fast lock feature.

The use of fractional-N synthesizers also allows low cost external parts to be used (i.e., VCO, resistors, and capacitors in the loop filter). Since VCO noise is suppressed within the loop bandwidth, wide loop bandwidth means VCO parts with high phase noise can be used without affecting the overall phase noise performance at the synthesizer output. Due to a high reference frequency, the various current leakages, as previously discussed, are no longer a concern. This means that low-leakage capacitors are not necessary.

Performance Parameters of Fractional-N Synthesizers and Related Design Issues

Some of the benefits provided by fractional-N synthesizers are not fully realized depending on the architecture used. There are potential performance deviations from the applied use of fractional-N synthesizers from the ideal case. If an appropriate fractional-N synthesizer is selected, these potential deviations can be minimized.

Fractional Spurs

These spurs appear at an offset frequency of $0.F f_{ref}$, and possibly its harmonics, where $0.F$ is the fractional part of the division ratio. They occur in pairs (i.e., if it appears at an offset frequency f_0, it will be seen at $-f_0$ as well). Also, the pair of spurs at $\pm 0.F f_{ref}$ tend to be the highest. The behavior of fractional-N spurs are quite different between $\Delta\Sigma$ fractional-N and non-$\Delta\Sigma$ fractional-N (i.e., current injection-based or fractional divider-based fractional-N).

Fractional Spurs in ΔΣ Fractional-N Synthesizers

These spurs can be quite large within the loop bandwidth. For a given VCO frequency and, therefore, a fixed value of $0.F$, as higher offset frequencies are approached outside of the loop bandwidth, the spurs are suppressed significantly or are even completely gone. When the fractional spurs are moved away from the carrier by varying $0.F$, they also decrease in size. Either way, the spurs

appear to be attenuated quite effectively by the low-pass action of the loop, as in the case with phase noise on the reference.

To evaluate the performance on fractional spurs, it is advisable to place the fractional spurs as close to the carrier as possible and then gradually move them to higher offset frequencies outside the loop bandwidth. This can be done by choosing a VCO frequency close to an integer boundary of f_{ref} and then gradually moving the carrier away from the boundary. Note that one of the two highest spurs occurs at an integer boundary. This is because the boundary is $0.Ff_{ref}$ away from the carrier.

The spur performance of ΔΣ fractional-N can be characterized by two parameters: the size of spurs within the loop bandwidth and how quickly they are attenuated as they are moved out of the loop bandwidth towards high offset frequencies. These two parameters determine the ratio of low spur to high spur bands of synthesized frequencies for a given application or standard. Figure 10 helps to explain this.

The high spur bands (area C in Figure 10) are centered at each integer-N boundary. In a high spur band, the synthesizer output has high spurious content close to the carrier (e.g., –55 dBc at a 10 kHz offset frequency). This area may or may not be useful, depending on the application. In the low spur band (area A in Figure 10), fractional spur levels meet the desired specifications or are below the phase noise floor. In area B of Figure 10, the spur level transitions from the low spur region to the high spur region at a rate of *x* dB/dec, which is determined by the closed-loop transfer function of the PLL.

For example, if a given application used a 20 MHz reference and a 20 kHz PLL loop bandwidth, and it was determined that the spur levels inside the loop bandwidth at integer-N boundaries were too high, the percentage of usable bandwidth, which meets the spurious specification for the application, would be:

$$\frac{20 - 0.02}{20} \times 100 = 99.9\%$$

A number of factors are thought to be the possible causes of fractional spurs in ΔΣ fractional-N. These include the operation of the ΔΣ modulator, the coupling between the PD/CP and the outside world through the power supply line or substrate, the nonlinearity of the charge pump, and divider kick-back to the VCO.

Fractional Spurs in Non-ΔΣ Fractional-N Synthesizers

With non-ΔΣ fractional-N synthesizers, the spurs tend to appear in the entire frequency range between two adjacent integer boundaries of f_{ref}. In this case, the primary cause for the spurs is the imperfect quantization phase error cancellation due to using fractional frequency division or current injection.

Degradation of The PD/CP Noise Floor

One of the advantages of fractional-N synthesis is its low phase noise as a result of high f_{ref} and, therefore, a small frequency division ratio *N.F*. Based on Equation 3, this is true only if the PD/CP noise floor is kept at the same level. In reality, the part of circuitry included in a fractional-N synthesizer to realize fractional-N frequency synthesis can cause this noise floor to rise. The degree of PD/CP noise floor degradation depends on the architecture used and on circuit implementation.

In current injection-based fractional-N, any noise on the compensation current can increase the noise floor. In fractional divider-based fractional-N, phase noise on the output of the delay stages in the delay line can be a primary reason for an increase in the noise floor.

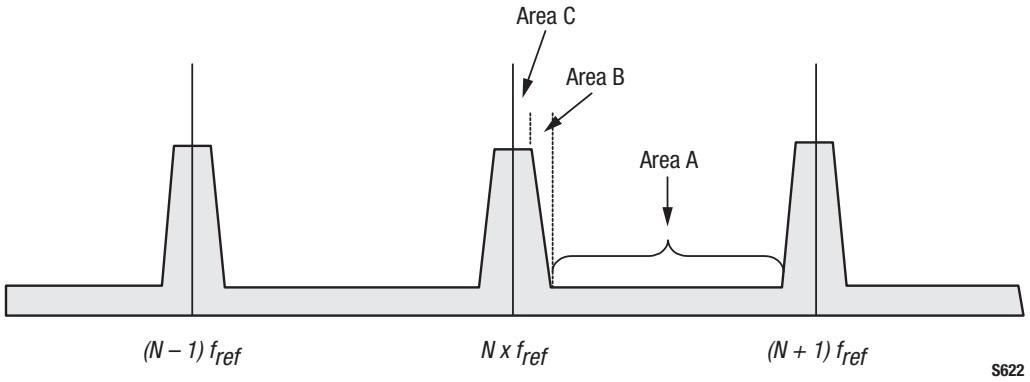

Figure 10. High Spur Bands

In the case of ΔΣ fractional-N, nonlinearity in the PD/CP may give rise to a significant noise floor increase. The nonlinearity causes the high-frequency quantization noise to be mixed down into the baseband. This actually poses an additional constraint in the PD/CP design for ΔΣ fractional-N synthesizers. That is, designers need to worry about linearity and noise at the same time.

It is a straightforward matter to find out whether or not the PD/CP noise floor is degraded by fractional division, provided that the fractional-N synthesizer also supports an integer-N operation mode. This can be done by switching between fractional-N and integer-N modes and noting the difference in phase noise. This difference is a measure of the noise floor degradation. If there is no degradation, the design has been successful. The integer division ratio used in the integer-N mode should be close to the non-integer division ratio. In this way, the variation on phase noise floor due to the frequency division ratio change can be ignored.

Fractionality

In non-ΔΣ fractional-N, fractionality is given as a set of fractional moduli or fractional denominators. For example, if 15 is given as one of the supported fractional moduli, the fractional part of the non-integer division ratio can be 1/15, 2/15, 3/15, … 14/15.

In ΔΣ fractional-N, fractionality is characterized by the number of bits in the input to the ΔΣ modulator. For example, if the modulator is 20-bit, then the fractional part of the division ratio is given by *k*/220, where *k* is an integer number between 1 and 220–1.

In the language of non-ΔΣ fractional-N, the fractional modulus supported is $1/2^{20}$. The fractionality should be high enough (i.e., the supported fractional denominator is large enough) to achieve the desired step size and the phase noise floor at the same time. Otherwise, the trade-off between the step size and the phase noise floor, as with traditional integer-N, is still present.

Also, fractionality should be appropriate for the crystal frequency used and the application. This is not a concern, however, if the fractional-N synthesis is based on a ΔΣ modulator and if the number of bits in the modulator is sufficiently large.

Tuning Speed

It is often thought that tuning speed is not a concern with fractional-N synthesis. However, if fractionality is not high enough to require the use of a low reference frequency, the resulting narrow bandwidth may yield a slow tuning speed. However, this is probably not the case with ΔΣ fractional-N synthesizers where fractionality can be easily increased.

In this case, the need to suppress quantization noise restricts the loop bandwidth to some reasonable portion of f_{ref}, which sets a practical limit on the tuning speed. However, as f_{ref} can be in the order of tens of MHz, in general, the tuning speed is much higher than that for integer-N synthesizers.

List of Selection Criteria Unique to Fractional-N

The following criteria, and the criteria applicable to integer-N synthesizers, are important to keep in mind when selecting a fractional-N supplier:

- The type of fractional-N synthesizer (i.e., is it a ΔΣ fractional-N or non-ΔΣ fractional-N?).
- The magnitude of in-band fractional spurs, the ratio of usable band over non-usable band, and temperature and supply voltage dependence of the fractional-N spurs.
- The degree of CP/PD noise floor degradation and whether it is dependent on temperature.
- Fractionality. Is it sufficient to deliver the required step size, the desired speed, and phase noise floor at the same time?
- Power consumption increase needed to realize fractional-N frequency synthesis.
- Maximum reference frequency allowed.

The type of fractional-N synthesizer chosen is important because the spur behavior, the degree of CP/PD noise degradation, and the fractionality could be quite different between the two types of fractional-N synthesis.

Summary

Fractional-N synthesizers allow the frequency step size to be a fraction of the reference frequency. This makes it possible to achieve low phase noise, small step size (ppm), fast tuning speed, and minimal reference feedthrough spurs at the same time.

There are a number of ways to achieve fractional-N frequency synthesis. So far, ΔΣ modulator-based fractional-N synthesizers have emerged as the most successful technique to achieve all performance requirements at once. The high quantization noise at high frequencies can be readily filtered out by the low-pass filtering function of the loop.

Fractional spurs can still be a problem in ΔΣ fractional-N synthesizers, but normally this problem persists only over very narrow and predictable bands. Together with other performance parameters, this should be examined when it comes to selecting a fractional-N supplier.

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